CLAIMS

1. In a device providing an output signal, an apparatus for generating output clock pulses for the output signal, comprising:

a clock generator producing an output clock signal having periodic cycles with leading and following edges;

an output clock pulse forming circuit, coupled to the output clock generator, which produces output clock pulses for corresponding output clock cycles in response to the leading and following edges of the output clock cycles and a relative phase of transitions of the output signal and the leading edges of the output clock cycles.

2. The apparatus of claim 1, wherein the output clock pulse forming circuit includes:

circuitry to generate a leading edge of the output clock pulse upon the leading edge of the corresponding output clock cycle if the transition of the output signal occurs before the leading edge of the corresponding output clock cycle, and upon a transition of the output signal if the transition of the output signal occurs after the leading edge of the corresponding output clock cycle; and

circuitry to generate a following edge of the output clock pulse upon an following edge of the corresponding output clock cycle if the transition of the output signal occurs before the leading edge of the corresponding output clock cycle, and upon an edge of a delayed output clock signal if the transition of the output signal occurs after the leading edge of the corresponding output clock cycle.

3. The apparatus of claim 1, including:

a memory including memory cells, and having address/data paths and timing paths which emulate the address/data paths, the address/data paths outputting said output signal in response to addresses and the timing paths outputting dummy data in response to an address emulation signal; and

an output clock phase detector coupled to the clock generator, to the output clock pulse forming circuit, and to the timing paths of the memory, which generates signals

indicating the relative phase of transitions of the output signal and the leading edges of the output clock cycles in response to the dummy data and the output clock cycles.

4. The memory device of claim 1, including

a memory including memory cells, and having address/data paths and timing paths which emulate the address/data paths, the address/data paths outputting said output signal in response to addresses and the timing paths outputting dummy data in response to an address emulation signal; and

an output clock phase detector coupled to the clock generator, to the output clock pulse forming circuit, and to the timing paths of the memory, which generates signals indicating the relative phase of transitions of the output signal and the leading edges of the output clock cycles in response to the dummy data and the output clock cycles; wherein

the clock generator generates a sense enable signal supplied to the memory, and having a period substantially equal to the output clock cycles, and said memory comprises a plurality of memory banks, memory banks having respective sense amplifiers responsive to said sense enable signal, and said address/data path comprises

address path spines which extend in a first direction among said plurality of memory banks, address path ribs that extend orthogonally with respect to said address path spines, and decoding circuitry for enabling portions of said address path spines and address path ribs for access to addressed memory banks; and

data path spines which extend in said first direction adjacent said memory banks and to output structures for data from the memory, and data path ribs among said memory cell blocks which extend orthogonally with respect to said first direction from sense amplifiers in said plurality of memory banks to said data path spines;

wherein said timing paths are co-located with said address path spines, address path ribs, data path ribs and data path spines.

5. The memory device of claim 1, including output structures to output the output signal, and wherein said output structures are responsive to said output clock pulses.

6. The memory device of claim 1, including output structures to output the output signal, and wherein said output structures output an echo clock in response to said output clock pulses.

7. The apparatus of claim 1, wherein the clock generator comprises adjustable circuitry to adjust the relative phase of said output clock cycles in response to the relative phase of transitions of the output signal and the leading edges of the output clock cycles.

8. The apparatus of claim 1, including:

an output clock phase detector coupled to the clock generator, to the output clock pulse forming circuit, and to the timing paths of the memory, which generates signals indicating the relative phase of transitions of the output signal and the leading edges of the output clock cycles; wherein

the clock generator comprises adjustable circuitry to dynamically adjust the relative phase of said output clock cycles in response to the relative phase of transitions of the output signal and the leading edges of the output clock cycles.

9. A memory device in which output data is supplied on an output in an output clock cycle within a read latency of more than one output clock cycle, comprising:

a memory including a set of blocks of memory cells, the members of said set of blocks having respective address/data paths and respective timing paths collocated with the address/data paths, the address/data paths outputting data for the respective blocks in response to addresses and the timing paths outputting dummy data for the respective blocks in response to an address emulation signal;

a set of clock channels having respective inputs and outputs;

a clock generator, responsive to an input clock, producing an output clock signal having said output clock cycles with an adjustable phase and a dummy data reference clock signal on the inputs of clock channels in the set of clock channels, and producing an address emulation signal on the timing paths for the blocks in the memory, the address emulation signal and the dummy data reference clock signal having substantially equal periods that are a multiple of the output clock cycle long;

clock control logic coupled to the clock generator that adjusts the adjustable phase of the output clock signal on the inputs of clock channels in the set of clock channels; and

an output clock pulse forming circuit, coupled to the output of the clock channels, which produces output clock pulses for corresponding output clock cycles in response to the leading and following edges of the output clock cycles and a relative phase of transitions of the dummy data and the leading edges of the output clock cycles.

10. The memory device of claim 9, wherein the output clock pulse forming circuit includes:

circuitry to generate a leading edge of the output clock pulse upon the leading edge of the corresponding output clock cycle if the transition of the output signal occurs before the leading edge of the corresponding output clock cycle, and upon a transition of the output signal if the transition of the output signal occurs after the leading edge of the corresponding output clock cycle; and

circuitry to generate a following edge of the output clock pulse upon an following edge of the corresponding output clock cycle if the transition of the output signal occurs before the leading edge of the corresponding output clock cycle, and upon an edge of a delayed output clock signal if the transition of the output signal occurs after the leading edge of the corresponding output clock cycle.

11. The memory device of claim 9, wherein said memory cells comprise thyristor-based memory cells.

12. The memory device of claim 9, wherein the clock generator generates a sense enable signal supplied to the memory, and having a period substantially equal to the output clock period, and said memory blocks comprise respective pluralities of memory banks, memory banks having sense amplifiers responsive to said sense enable signal, and said address/data path comprises

address path spines which extend in a first direction among said plurality of memory banks, address path ribs that extend orthogonally with respect to said address

path spines, and decoding circuitry for enabling portions of said address path spines and address path ribs for access to addressed memory banks; and

data path spines which extend in said first direction adjacent said memory banks and to output structures for data from the memory, and data path ribs among said memory banks which extend orthogonally with respect to said first direction from sense amplifiers in said plurality of memory banks to said data path spines;

wherein said timing paths for said address emulation signal and said dummy data are co-located with said address path spines, address path ribs, data path ribs and data path spines.

13. The memory device of claim 9, including output structures to output data accessed from the plurality of memory blocks, and wherein said output structures are responsive to said output clock pulses.

14. The memory device of claim 9, including output structures to output data accessed from the plurality of memory blocks, and wherein said output structures output an echo clock in response to said output clock pulses.

15. For a device providing an output signal, method for generating output clock pulses for the output signal, comprising:

generating an output clock signal on the device, the output clock signal having periodic cycles with leading and following edges;

forming output clock pulses for corresponding output clock cycles on the device in response to the leading and following edges of the output clock cycles and a relative phase of transitions of the output signal and the leading edges of the output clock cycles.

16. The method of claim 15, wherein forming the output clock pulse includes:

generating a leading edge of the output clock pulse upon the leading edge of the corresponding output clock cycle if the transition of the output signal occurs before the leading edge of the corresponding output clock cycle, and upon a transition of the output

signal if the transition of the output signal occurs after the leading edge of the corresponding output clock cycle; and

generating a following edge of the output clock pulse upon an following edge of the corresponding output clock cycle if the transition of the output signal occurs before the leading edge of the corresponding output clock cycle, and upon an edge of a delayed output clock signal if the transition of the output signal occurs after the leading edge of the corresponding output clock cycle.

17. The method of claim 15, wherein said device comprises a memory including memory cells, and having address/data paths and timing paths which emulate the address/data paths, the address/data paths outputting said output signal in response to addresses and the timing paths outputting dummy data in response to an address emulation signal; and including

generating signals indicating the relative phase of transitions of the output signal and the leading edges of the output clock cycles in response to the dummy data and the output clock cycles.

18. The method of claim 17, wherein said memory cells comprise thyristor-based memory cells.

19. The method of claim 15, including latching the output signals in response to said output clock pulses.

20. The method of claim 15, including supplying an echo clock in response to said output clock pulses at an output of the device.